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Micromachined circuits for Mm-wave applications

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Abstract

A novel transmission line which utilizes micromachining techniques in the development of circuits for millimeter-wave applications is presented. Micromachined circuits incorporate the fabrication of an upper-half shielding environment with the circuit geometry. The circuit development requires the use two silicon wafers where one has cavities that have been etched using anisotropic etching while the other one has the planar circuits which have been printed using standard photolithographic techniques. Afterwards, the two wafers are aligned and secured using bonding techniques to form a circuit that has an upper-half shielded cavity incorporated monolithically. This paper presents a detailed description the fabrication procedure necessary for upper-half shielded (UHS) circuits as well as for completely shielded (CS) circuits. Experimental results of the upper half shielded circuits will be presented as compared to theoretical results and conventional coplanar waveguide circuits of the same type.

Introduction

Uniplanar transmission lines, such as microstrip, coplanar waveguide and slotline have provided enhanced flexibility in high-frequency circuit design, reduced weight and volume, and compatibility to high-speed active devices. Planarization, however, gives rise to unwanted frequency dependent mechanisms such as parasitic coupling and radiation which deteriorate electrical performance and lead to costly and time intensive design cycles. Suppression of these electromagnetic mechanisms has led to improved performances but has required very sophisticated packages which considerably add to the volume, weight and most important cost of the circuits. Consequently, the development of new packaging techniques which minimize cost and reduce volume and weight can have a major impact in today's technology and can lead to high volume markets.

This paper presents the development of miniaturized circuits of coplanar waveguide type where the package has been fabricated and integrated with the rest of the circuit using Si-based Micromachining [1],[2]. The characterization of these circuits has been completed both theoretically and experimentally with very close agreement between theory and experiment. In the following sections the fabrication process of micromachined circuits is described and theoretical as well as experimental data are presented and discussed for a variety of three-dimensional structures.

Fabrication

Micromachined circuits, consisting of conducting lines and metallized cavities, are developed in two stages using a two-wafer system. In this section a comprehensive discussion is presented on the development of completely shielded as well as upper-half shielded micromachined circuits. First, the cavity structure, Figure 1, is etched into a low resistivity Si wafer (353μm) having a 1.4μm dielectric tri-layer of oxide/nitride/oxide. This wafer requires the production of alignment marks which are etched through the entire wafer along with cavities which are etched through partially. In this process, the areas to be etched are defined using standard photolithographic techniques. Since the tri-layer must be removed in the areas of silicon to be etched, the upper oxide layer is etched using buffered HF while the middle nitride layer is etched by a plasma etcher. The wafer is then repatriated to expose and remove the lower oxide layer in the areas that will be etched entirely while preserving the lower oxide layer in the areas that will be etched partially.

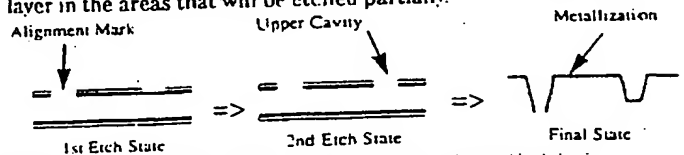

FIGURE 1. Development of cavity regions on the upper wafer for Micromachined circuits.

Since the tri-layer dielectric is used as a mask when anisotropically etching, KOH or EDP, the initial desired depth is etched into the silicon surface. Next, the remaining lower oxide layer in the cavity areas are removed using buffered HF and the wafer is etched for the remaining depth to produce both the alignment windows and appropriate cavity depth.

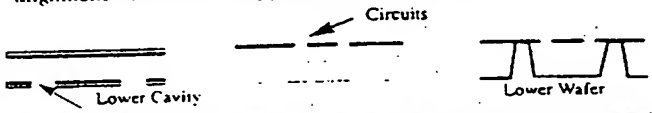

FIGURE 2. Development of cavity regions and circuits on the lower wafer for the Micromachined circuits.

Second, for the development of completely shielded circuits, cavities must be incorporated below the surface of the circuit layer. This is done by anisotropically etching grooves in the backside of a high resistivity Si wafer (353μm) having the tri-layer dielectric mask as described above. Next, planar CPW-like geometries are printed, using photolithographic and metal evaporation techniques for a liftoff procedure. Once complete, the cavity structure is then metallized using evaporation techniques.

FIGURE 3. Micromachined Completely Shielded and Upper-Half Shielded Circuit in two-dimensions.

Finally, alignment of the upper cavity to the planar circuits is obtained via microscope and the two wafers are attached using regular adhesion methods or Si-to-Si electrobonding. While the procedure described above concentrates on the development of completely shielded circuits, the upper-half shielded circuit follows the same procedure with the exclusion of the lower cavity etching step.

Results and Discussion

Measurement System:

The micromachined circuits were measured using an HP 8510B Network Analyzer system, which operates up to 40 GHz. Measurements are obtained from Cascade Microtech high frequency GSG probes via an Alessi probe station. In order to suppress parallel plate and microstrip modes between the circuits and the wafer chuck of the probe station, the circuit wafer is placed on 1/8" thick 5880 RT/ Duroid having ϵ_r=2.2. The Thru-Reflect-Line (TRL) calibration is performed to eliminate the effects of the connectors, cables, and probes from the measured data and to accurately establish a known reference plane for the various circuits. After calibrating, scattering parameter measurements of the circuits were obtained to compare theoretical and experimental data.

Circuit Description:

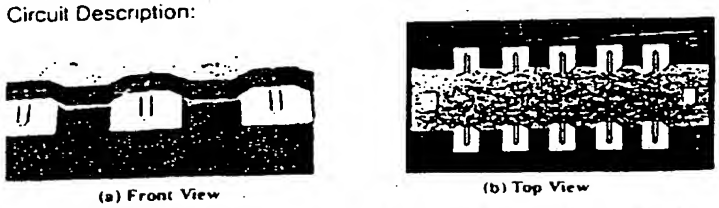

FIGURE 4. Micromachined Shielded CPW, Cavity Dimensions: height = 200 μm and width = 800 μm.

The circuits fabricated and tested are both open CPW and micromachined upper-half shielded CPW, as shown on Figure 4. The cavity region for these circuits are 800μm wide and 200μm high. Each circuit is fed by ungrounded open coplanar waveguide which has feed lines that transition from center conductor width of 100μm to 180μm and slot width of 60μm to 130μm. Since the TRL calibration is used, calibration standards were also fabricated to include identical cpw feed line to shielded region transitions for accurate calibration of the micromachined circuits.

Measurement Results:

The experimental results shown are for the micromachined upper-half shielded (UHS) circuit. Initial characterization is obtained by measuring the scattering parameters of a through line where the performance characteristics are extracted. Below in Figure 5 is a graph that shows the total loss of the through line, where the loss per guided wavelength is about 0.08 dB/λg.

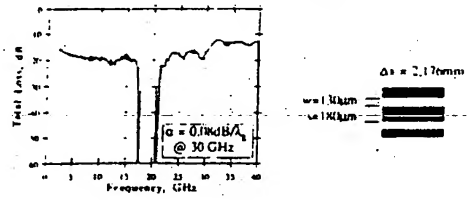

FIGURE 5. Through line characteristics for the Micromachined Upper-Half Shielded CPW.

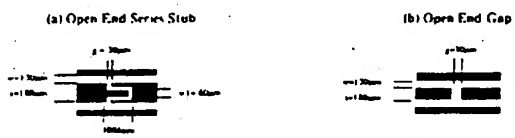

FIGURE 6. Circuit description for the (a) Open End Series Stub and the (b) Open End Gap.

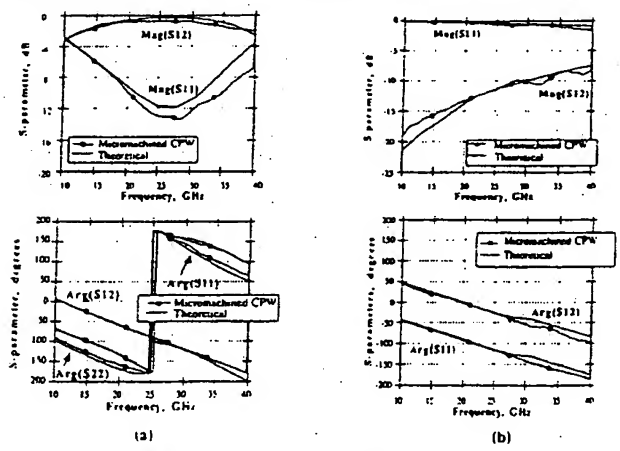

FIGURE 7. Micromachined UHS CPW: Theoretical vs. Experimental: (a) Open End Series Stub and (b) Open- End Gap

Various circuits were measured as part of this characterization effort which include an open-end series stub, designed to resonate at 30 GHz, and an open-end gap as shown above in Figure 6. Figure 7 shows a comparison between theoretical and experimental data for the micromachined UHS open-end series stub and open-end gap respectively. The theoretical results were derived using a full-wave spacedomain integral equation technique [3] and agree very well with the experimental results in both the magnitude and phase. Figure 8 shows a comparison between experimental data for the micromachined UHS CPW and

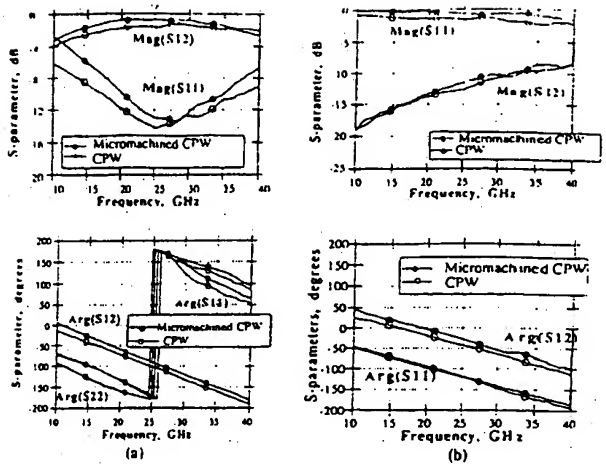

FIGURE 8. Micromachined UHS CPW vs. CPW: (a) Open End Series Stub and (b) Open End Gap.

open CPW in the case of the open end series stub and open end gap circuits. The results indeed verify that the micromachined cavity does not affect the electrical performance of the planar circuit.

Similarly, Figure 9 below shows experimentally measured total loss for the open end series stub and open end gap. The total loss is reduced by an average of 3 dBs from 10 to 40 GHz for the micromachined UHS CPW as compared to the open CPW. This reduction is due to elimination of radiation in the upper-half region of the circuit and emphasizes the effectiveness of the integrated cavity. Although the primary focus has been on the upper-half shielded circuits, some experimental results for the completely shielded geometries will be presented at the conference.

Conclusion

In conclusion, we have presented the development of micromachined circuits of simple geometries. The fabrication has been shown for both the completely shielded and upper-half shielded circuits. Comparisons have been shown between the upper-half shielded circuits and theory as well as open CPW measurements. Thus, with the improvement of the above loss performance combined with smaller volume and lower weight, micromachined circuits indeed make a very good candidate for development of integrated microwave and millimeter-wave packages.

Acknowledgments

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References

1. M. Yap, Y-C Tai, W.R. McGrath and C. Walker, "Silicon Micromachined Waveguides for Millimeter and Submillimeter Wavelengths," presented in the 3rd International Symposium on Space Terahertz Technology. Ann Arbor, MI. March 1992.

2. Linda P.B. Katehi," Low-Loss Transmission Lines for Terahertz Frequency Applications," IEEE Proceedings, November 1992, pp. 1771-1787.

3. N.I. Dib, L.P.B. Katehi, G.E. Ponchak and RN. Simons, "Theoretical and Experimental Characterization of Coplanar Waveguide Discontinuities for Filter Applications, IEEE Trans. on MTT, Vol. 39, No. 5. May 1991.

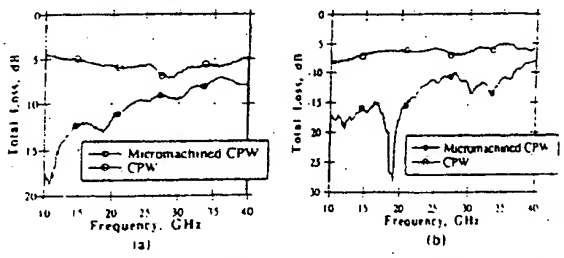

FIGURE 9. Micromachined UHS CPW vs. CPW Total Loss: (a) Open End Series Stub and (b) Open End Gap